IN THE ABSTRACT

Please replace the Abstract of the Disclosure currently on file with the attached substitute Abstract.

Abstract

A semiconductor integrated circuit device having a mechanism of compensating not only circuit operational speed but also variations in leakage current, which includes: a main circuit constructed with CMOS device, a delay monitor for simulating a critical path of the main circuit constructed by a CMOS and monitoring a delay of the path, a PN Vt balance compensation circuit for detecting a threshold voltage difference between a PMOS transistor and an NMOS transistor, and a well bias generating circuit for receiving outputs of the delay monitor and the PN Vt balance compensation circuit and applying a well bias to the delay monitor and the main circuit so as to compensate the operation speed of the delay monitor to a desired speed and reduce a threshold voltage difference between the PMOS and NMOS transistors.